In the Claims:

1-23. Cancelled

24. (Previously Presented) A method of forming a semiconductor device, the method comprising:

forming a cell gate oxide in a cell region;

forming a logic gate oxide in a periphery region;

forming a first doped polysilicon layer on the cell gate oxide; and

forming a second polysilicon layer, the second polysilicon layer being in contact with the logic gate oxide in the periphery region and in contact with a major surface of the first doped polysilicon layer in the cell region;

wherein the logic gate oxide and the first doped polysilicon layer form a first transistor and the cell gate oxide, the first doped polysilicon layer, and the second polysilicon layer form a second transistor.

25. (Original) The method of claim 24 wherein the second polysilicon layer positioned above the cell gate oxide is a p-type doped polysilicon.

26. (Original) The method of claim 25 wherein the second polysilicon layer is doped with a material selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony.

27. (Previously Presented) The method of claim 24 wherein the step of forming a first doped polysilicon layer is performed by depositing by furnace an in-situ doped polysilicon.

28. (Original) The method of claim 27 wherein depositing by furnace is performed at a temperature of about 540° C to about 640° C.

29. (Original) The method of claim 24 wherein the second polysilicon layer is formed of undoped polysilicon.

30. (Original) The method of claim 24 further comprising the step of doping the second polysilicon layer located above the cell gate oxide with a p-type dopant.

31. (Original) The method of claim 30 further comprising the step of doping the second polysilicon layer located above the logic gate oxide with an n-type dopant.

32. (Original) The method of claim 30 further comprising the step of doping the second polysilicon layer located above the logic gate oxide with a p-type dopant.

33. (Original) The method of claim 30 wherein the p-type dopant is selected from the group consisting essentially of phosphorous, nitrogen, arsenic, and antimony.

34. (Withdrawn-currently amended) A method of forming a semiconductor device, the method comprising:

forming a gate oxide in a first region and a second region;

forming at least one or more conductive gate layers on the gate oxide in the first region and the second region; and

forming one or more additional conductive gate layers over the one or more conductive gate layers in the second region;

wherein the gate oxide and the one or more conductive gate layers in the first region form a first transistor and the gate oxide, the one or more conductive gate layers, and the one or more additional conductive gate layers in the second region form a second transistor.

35. (Withdrawn-currently amended) The method of claim 34, wherein at least one of the additional conductive gate layers positioned above the ~~cell~~ gate oxide comprises a p-type doped polysilicon.

36. (Withdrawn) The method of claim 34, wherein the forming one or more additional conductive gate layers is performed at least in part by depositing by furnace an in-situ doped polysilicon.

37. (Withdrawn) The method of claim 36, wherein depositing by furnace is performed at a temperature of about 540° C to about 640° C.

38. (Withdrawn) The method of claim 34, wherein at least one of the additional conductive gate layers is formed of undoped polysilicon.

39. (Withdrawn) A method of forming a semiconductor device, the method comprising:

forming a gate oxide in a first region and a second region; and

forming a conductive gate layer on the gate oxide in the first region and the second region, the conductive gate layer comprising one or more layers of a conductive material, the conductive gate layer in the first region having fewer layers than the conductive gate layer in the second region;

wherein the gate oxide and the conductive gate layer in the first region form a first transistor in the first region and the gate oxide and the conductive gate layer form a second transistor in the second region.

40. (Withdrawn) The method of claim 39, wherein at least one of the layers comprises a p-type doped polysilicon.

41. (Withdrawn) The method of claim 39, wherein the forming the conductive gate layer is performed at least in part by depositing by furnace an in-situ doped polysilicon.

42. (Withdrawn) The method of claim 41, wherein depositing by furnace is performed at a temperature of about 540° C to about 640° C.

43. (Withdrawn) The method of claim 39, wherein at least one of the layers is formed of undoped polysilicon.